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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,664	12/12/2001	Christophe Chevallier	400.069US01	7828

7590 04/13/2004

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EXAMINER	
NGUYEN, VIET Q	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/017,664	Applicant(s) CHEVALLIER, CHRISTOPHE	
	Examiner Viet Q Nguyen	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Election filed on 1/26/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,38 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,11,15-17,38 and 39* is/are rejected.

7)☒ Claim(s) *9,10,12-14 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/12/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The applicant's election of Group I, claims **1-18 and 38-39** are acknowledged.

Claims **1-18** and **38-39** are present for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1-3, 5-8, 11, 15-17, and 38** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chang et al (5,894,437).**

Chang et al (see Fig.1) teaches a flash memory device comprising a plurality of bit lines (LBL) and a plurality of global bit lines (GRBL or GWBL) for separate read and write memory accesses. In Fig.1, fro example, ***a particular set of adjacent local bit lines could have been formed by the two shown local bit lines (LBL00) and (LBL10) which are also adjacent to each other***. However, there are also shown two separated select transistors (18), each transistor is for such local bit line (15), ***to be connected to one of the separated and different global bit lines*** (GRBL0 or GRBL1) as claimed. Further, its would be obvious from the drawing that the shown row lines (16) also act as the claimed select

lines for activating the control gates of these select transistors (18) coupled to the local bit lines as recited.

Regarding claim 3, there are shown at least 3 adjacent local bit lines as recited which could have included a plurality of such local bit line arrangements if desired (read cols.2-3).

3. Claims **1-8, 11, 15-17, and 38-39** rejected under 35 U.S.C. 103(a) as being unpatentable over **Tedrow et al (US 2002/0085423 A1).**

Tedrow et al (see Fig.2) shows a plurality of local bit lines and plurality of global bit lies in which each select transistor for each local line is used to couple to a different global bit line as recited, and the shown "local Y selects" lines act as the claimed "select lines" for activating the control gates on the said select transistors as desired. Furthermore, it would have been obvious that the number of adjacent local bit lines could be two or more since Fig. 7A and 7B also shows two separated sets of local bit lines (in each block) ***where each set contain even number or odd number of bit lines depending on their block locati***on, thus obviously meet claims 3 and 4 limitations.

4. Other claims contain allowable subject matter over prior arts of record.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Viet Q Nguyen whose telephone number is (571) 272-1788. The examiner can normally be reached on 7am-6pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Viet Q Nguyen
Primary Examiner
Art Unit 2818

V. Nguyen
4/5/04